UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,899	12/20/2001	Robert Alan Reid	01 P 09444 US	2160

7590 02/09/2006

Scott B. Stahl
Jackson Walker LLP
Suite 600
2435 N. Central Expressway
Richardson, TX 75080

EXAMINER	
BULLOCK JR, LEWIS ALEXANDER	
ART UNIT	**PAPER NUMBER**
2195	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,899	REID, ROBERT ALAN	
	Examiner	Art Unit	
	Lewis A. Bullock, Jr.	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-8, 11-17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by FLECK (U.S. Patent 6,128,641).

As to claim 1, FLECK teaches a method of switching from execution of a first data processing task (calling routine / function) to execution of a second data processing task (called routine / function), comprising: the first data processing task (calling routine / function) executing a call (call) to a task switching function (context switch control unit / instruction control unit); the task switching function selecting a return address (context / pointer to CSA) corresponding to the second data processing task (called routine / function); and the task switching function executing a return operation (context switch) (via allocating a CSA and updating the previous context save area list) (col. 1, lines 27-40; col. 1, line 57 – col. 2, line 32; col. 4, lines 10-30; col. 5, lines 49-67; col. 6, lines 17-20; col. 6, line 47 – col. 7, line 28).

As to claim 11, FLECK teaches an apparatus for switching from execution of a first task (calling routine / function) on a data processor (data processing unit) to execution of a second task (called routine / function) on the data processor, comprising:

a memory (memory) having a first storage location for storing a return address corresponding to the second task (via storing CSA on previous context save area list); an input (call) for receiving information indicative of instructions of a task switching function that has been called by the first task (via the calling routine making a call for a called routine); and a memory management apparatus (via the context switch control unit) coupled to the input and the memory, and responsive to the instruction information indicating a return instruction for moving the return address from the first storage location to a register of the data processor (via performing a context switch thereby saving the CSA and creating a new one or returning to a previous CSA) (col. 1, lines 27-40; col. 1, line 57 – col. 2, line 32; col. 4, lines 10-30; col. 5, lines 49-67; col. 6, lines 17-20; col. 6, line 47 – col. 7, line 28).

As to claim 17, FLECK teaches a data processing apparatus, comprising: a data processing portion for executing first and second data processing tasks (data processing unit); a task switcher (context switch control unit) coupled to the data processing portion for switching from execution of the first task (calling routine / function) to execution of the second task (called routine / function), the task switcher including a memory (memory) having a storage location for storing a return address corresponding to the second task (via storing CSA on previous context save area list), and an input for receiving information indicative of instructions of a task switching function that has been called by the first task (via the calling routine making a call for a called routine); a register coupled to the task switcher (data registers / address

registers); and the task switcher including a memory management apparatus coupled to the input and the memory; and responsive to the instruction information indicating a return instruction for moving the return address from the storage location to the register (via performing a context switch thereby saving the CSA and creating a new one or returning to a previous CSA) (col. 1, lines 27-40; col. 1, line 57 – col. 2, line 32; col. 4, lines 10-30; col. 5, lines 49-67; col. 6, lines 17-20; col. 6, line 47 – col. 7, line 28).

As to claim 2, FLECK teaches the selecting step includes the task switching function selecting a first pointer (address / pointer) that points to a first area of memory (CSA) where the return address is stored (col. 5, lines 49-67; col. 6, lines 9-12; col. 6, lines 47-54).

As to claim 3, FLECK teaches the pointer selecting step includes updating a second pointer to point to the first pointer (via saving a CSA to the list or restoring a CSA from the list / read-write-modify operation) (col. 6, lines 21-30).

As to claim 4, FLECK teaches the updating step includes updating the second pointer from a status wherein the second pointer points to a third pointer to a status wherein the second pointer points to the first pointer, and wherein the third pointer points to a second area of memory (via saving a CSA to the list or restoring a CSA from the list / read-write-modify operation) (col. 6, lines 21-30).

As to claim 5, FLECK teaches a return address corresponding to the first data processing task (calling function / routine) is stored in the second area of memory (via the second portion of the CSA which stores a pointer to another CSA / via following the list to the previous CSA) (col. 5, lines 49-61; col. 7, lines 10-28).

As to claim 6, FLECK teaches the task switching function storing the third pointer (via context switching functions thereby storing CSAs to the list) (col. 1, lines 27-40; col. 1, line 57 – col. 2, line 32; col. 4, lines 10-30; col. 5, lines 49-67; col. 6, lines 17-20; col. 6, line 47 – col. 7, line 28).

As to claim 7, FLECK teaches the task switching function deselecting a return address (pointer / address) corresponding to the first data processing task (via restoring the calling function / routine from the linked list) (col. 2, lines 7-21).

As to claim 8, FLECK teaches saving a return address (pointer / address) corresponding to the first data processing task (calling routine / function) (via switching context based on call) (col. 4, lines 10-30), and executing the saving step in parallel with the call executing step (col. 4, lines 49-55).

As to claim 12, FLECK teaches memory includes a second storage location for storing a first pointer (address / pointer) which points to a first area of the memory (CSA) that includes the first storage location, the memory management apparatus

responsive to the instructions information for selecting the first pointer (via chaining addresses of CSAs to the list or using the list restore chained addressed CSAs on the list) (col. 1, lines 27-40; col. 1, line 57 – col. 2, line 32; col. 4, lines 10-30; col. 5, lines 49-67; col. 6, lines 17-20; col. 6, line 47 – col. 7, line 28).

As to claim 13, FLECK teaches the memory management apparatus includes a memory manager for maintaining a second pointer (address / pointer), the memory manager responsive to the instruction (context switch / restore) information for updating the second pointer to point to the first pointer in the memory (via updating the listed chained addressed CSAs after appending or removing CSA's to the list / read-write-modify operation) (col. 1, lines 27-40; col. 1, line 57 – col. 2, line 32; col. 4, lines 10-30; col. 5, lines 49-67; col. 6, lines 17-30; col. 6, line 47 – col. 7, line 28).

As to claim 14, FLECK teaches the memory manager is operable for updating the second pointer from a status wherein the second pointer points to a third pointer stored at a third location in the memory to a status wherein the second pointer points to the first pointer, and wherein the third pointer points to a second area of the memory (via context switching functions thereby storing CSAs to the list) (col. 1, lines 27-40; col. 1, line 57 – col. 2, line 32; col. 4, lines 10-30; col. 5, lines 49-67; col. 6, lines 17-20; col. 6, line 47 – col. 7, line 28).

As to claim 15, FLECK teaches the second area of the memory (part of CSA / part of list element) includes a fourth storage location which stores therein a return address (address / pointer) corresponding to the first data processing task (calling routine / function) (via switching context based on call) (col. 4, lines 10-30).

As to claim 16, FLECK teaches the memory manager is responsive to the instruction information for storing the third pointer (address / pointer of subsequent listed CSAs) in the third location of the memory (via context switching based on a call to store the address of CSA on list and link with the previous CSA) (col. 1, lines 27-40; col. 1, line 57 – col. 2, line 32; col. 4, lines 10-30; col. 5, lines 49-67; col. 6, lines 17-20; col. 6, line 47 – col. 7, line 28).

As to claim 19, FLECK teaches the register is a program counter register (register) (col. 3, lines 21-32).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 10 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over FLECK (U.S. Patent 6,128,641).

As to claim 10, FLECK teaches executing a call to the task switching function (call instruction), the task switching function selecting a return address corresponding to a data processing task (via chaining addresses of CSAs to the list or using the list restore chained addressed CSAs on the list), and the task switching function executing a return operation (via returning from executing the previous task) (col. 1, lines 27-40; col. 1, line 57 – col. 2, line 32; col. 4, lines 10-30; col. 5, lines 49-67; col. 6, lines 17-20; col. 6, line 47 – col. 7, line 28). It would be obvious to one skilled in the art that the second task is a calling function / routine for a further called function.

As to claim 18, FLECK substantially discloses the invention above. However, FLECK does not teach the switcher includes TriCore data processor architecture. Official Notice is taken in that a Tri-Core data processor architecture is well known in the art and therefore would be obvious to one skilled in the art that the system of FLECK is implemented in a Tri-Core architecture in order to reduce execution overhead.

5. Claims 9 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over FLECK (U.S. Patent 6,128,641) in view of Applicant's Admitted Prior Art (APA).

As to claim 9, FLECK substantially discloses the invention above. However, FLECK does not teach the data processing task being a host task, disk task, or servo task. APA teaches that a data processing task is one of a host task, a disk task and a servo task of an optical drive control system (pg. 1, line 21 – 2, line 1). It would be obvious to one skilled in the art at the time of the invention to combine the teachings of

FLECK with the teachings of APA in order to switch firmware tasks more quickly than conventional microprocessors and microcontrollers (col. 4, lines 38-41; col .1, lines 27-31).

As to claim 20, FLECK substantially discloses the invention above. However, FLECK does not teach the data processing task being a host task, disk task, or servo task. APA teaches that a data processing task is one of a host task, a disk task and a servo task of an optical drive control system (pg. 1, line 21 – 2, line 1). It would be obvious to one skilled in the art at the time of the invention to combine the teachings of FLECK with the teachings of APA in order to switch firmware tasks more quickly than conventional microprocessors and microcontrollers (col. 4, lines 38-41; col. 1, lines 27-31).

Response to Arguments

6. Applicant's arguments filed November 16, 2005 have been fully considered but they are not persuasive. All of Applicant arguments are based on the same reasoning as detailed below. Applicant argues that Fleck either singly or in combination does not teach "selecting or storing a return address corresponding to the second data processing task" because if the called routine/function of Fleck is analogized to the second data processing task the CSA points to the previous context, i.e. the calling function, not the called function and thus does not select a return address of the called function. Applicant also states that the both the calling and called routines context must

be saved and then restored in order to resume either's execution after returning from a function. This is in contrast to the selecting of a return address corresponding to the second data processing task. The examiner disagrees. The claims as written detail switching execution from a first task to a second task by: the first task executing a call to a task switching function; the tasks switching function selecting a return address to the second task; and the task switching function executing a return operation. The fact that the first and second tasks context must be saved is irrelevant to the claim language as originally presented since the claims do not preclude one from storing both contexts. Fleck teaches its context switching function using a PCX field to point to the CSA for the previous context that will be restored when a respective return instruction is executed (col. 6, lines 46-54). To restore a context save area, the processor context to be restored is read from the CSA at the front of the previous context list such that the current head of the PCX is moved to the front of the FCX and the registers are updated such that the PCX points to the previous head, i.e. the calling routine (col. 7, lines 10-22). Hence, a first task (task associated with the current head of the PCX) executes a task switch call (via a store instruction or save context instruction), the task switching function selects a retun address corresponding to the second processing task (via moving the current context to the free list and updating the PCX to point to the former head); and the task switching function executing a return operation (via return instruction). Therefore, as detailed above the cited prior art adequately teaches the claims as disclosed and the rejection is maintained.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lewis A. Bullock, Jr. whose telephone number is (571) 272-3759. The examiner can normally be reached on Monday-Friday, 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER

February 6, 2006